Muhammad Hammad Bashir

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Professional Experience

10xEngineers | *Design Verification Engineer* Sep. 2023 – Present

- **Platform Level Verification for ARM to RISC-V Core Swap**
  - **Led a team of three** to develop a platform-level verification environment and test suite for replacing *ARM Cortex-A5* with *RISC-V Ariane* in the SSE-500 subsystem.
  - Designed the environment for the execution of RISC-V-based tests, which involved C- and assembly-level tests, and developed the boot flow for the swapped core.
  - Developed platform-level tests to verify interrupts, memory map, core configuration, and peripheral functionality.
  - Developed tests for the verification of the RISC-V platform-level interrupt controller (PLIC) and core-level interrupt controller (CLINT) within the RISC-V system.
- **RISC-V Compliance Verification – Open Source Contributions**
  - Led an 8-month project to enhance Privilege Architecture support in **RISC-V ISAC**, adding support for Virtual Memory and Physical Memory Protection. Additionally, developed a custom python-based translator to optimize the covergroup size, achieving a covergroup size reduction up to 50%.
  - Contributed to the *RISC-V Arch Tests* for the development of assembly tests and covergroups for multiple features of the RISC-V Privilege Specification including Physical Memory Protection, Virtual Memory, Interrupts, and Atomic extensions.
  - Added coverage support for timer and software interrupts and macros support in RISC-V ISAC and RISCOF.
- **RISC-V Certification Program**
  - Participating in the RISC-V Certification Tests and Model Working Group (WG) and Microcontroller WG.
  - Designed an in-house comprehensive test plan for RISC-V platform and SoC verification.

10xEngineers | *Subject Matter Expert* Mar. 2024 – Present

- Developed training material for Computer Architecture and RISC-V Architectural Tests Courses for the company's training program.

10xEngineers | *Associate Verification Engineer* Mar. 2023 – Aug. 2023

- Part of the team for the development of RISC-V architectural tests for Virtual Memory SV-32 page-based scheme for CVA6.
- Completed coursework in advanced Computer Architecture, RISC-V Architectural Tests Development and RISC-V assembly.

Research Publications

Posters

Muhammad Hammad Bashir, Umer Shahid, Allen Baum, Pawan Kumar Sanjaya, *Enhancing Privilege Architecture Support in RISC-V ISAC*, In **RISC-V Summit Europe**, Munich, Germany, 2024.

Talks and Tutorials

Tutorials

"Embedded Systems with RISC-V: Bare-Metal Firmware Development for CH32V003 Microcontrollers" in **RISC-V Community Event**, Lahore, Pakistan - November 2024.

Education

University of Engineering and Technology, Lahore Oct. 2020 – May 2024
Bachelor of Science in Electrical Engineering *CGPA: 3.41/4.0*

Technical Skills

Programming Languages: Python, System Verilog (HDL), C, bash scripting, Assembly Language (RISC-V & ARM), TCL scripting

Tools: Xilinx Vivado, VCS, Micro-vision Keil, ModelSim, QuestaSim, Git, GitHub, Visual Studio Code, Atom

RISC-V Compliance Verification Tools: RISCOF, RISC-V ISAC, RISC-V CTG, RISC-V Config

Architectural Simulators and Emulators: RISC-V Spike Model, RISC-V Sail Golden Model, QEMU

Operating Systems: Linux (Ubuntu), Windows