Verification of CoreSwap: Replacing ARM Cortex-A5 with RISC-V CVA6 in an ARM SoC Environment

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Abstract

This paper presents the verification methodology and results of the CoreSwap project, where the ARM Cortex-A5 core in ARM Educational Kit SoC was replaced with the open-source RISC-V OpenHW CVA6 core. This demonstrates the feasibility of integrating a RISC-V core into an existing SoC ecosystem while maintaining functionality and system stability. We detail the comprehensive verification process, including core-level Architecture Compliance Tests (ACTs), manually written system-level tests, FPGA synthesis on a Kintex-7 platform, and running performance benchmarks. This seamless integration and verification of the CoreSwap underscores the potential of RISC-V in proprietary SoC environments.

Methodology

The verification of coreswap was performed at multiple levels to ensure the correctness of the system including:

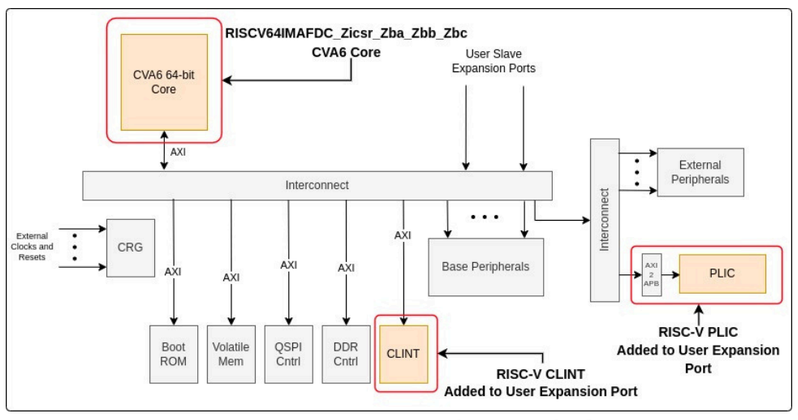
- **Core-Level Verification -** The CVA6 core's compliance with the RISC-V ISA was validated using the RISC-V Architecture Compliance Tests (ACT). It passed all mandatory ACT test cases, which checked correct execution of instruction and control-flow operations. The tests also confirmed proper handling of memory operations—loads and stores routed through the network interconnect—thereby ensuring both ISA adherence and correct system integration.
- **System-Level Verification -** System-level tests were run to validate the interaction between the CVA6 core and the SoC peripherals. These self-checking tests include the verification of the memory map, interrupt handling, and correct configuration setup. The following table summarizes a subset of the system-level test cases that we executed.

Test Case	Test Description	Test Target
Integration Sanity Test	Generic Test for the verification of correct boot flow and system initialization.	Whole System Integration
Memory Map Test	Verifies the correct memory configurations	Memory Map
Interrupts Test	Verifies the behavior of CLINT, PLIC including generation of timer, software and external interrupts with correct handling.	CLINT, PLIC, External Peripherals

Overview of Coreswap

Coreswap - The CoreSwap project involved replacing the ARM Cortex-A5 core with the RISC-V CVA6 core in an ARM Educational Kit SoC. The CVA6 core, an open-source, 64-bit RISC-V implementation, was chosen for its compatibility with the existing SoC infrastructure.

Interrupt Handling - Replaced ARM GIC with RISC-V PLIC to multiplex peripheral interrupts onto each HART's external interrupt lines and integrated CLINT to handle inter-processor interrupts and timer interrupt functionality. The complete block diagram is shown in Figure 1.



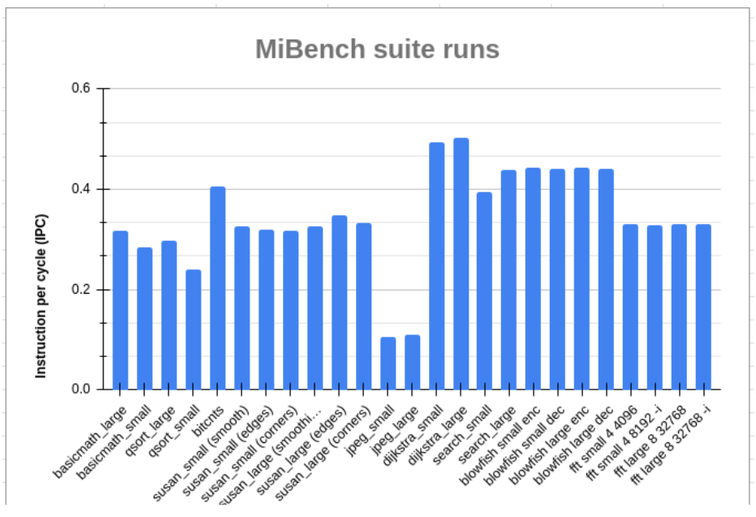
- *Figure 1 - Swapped Core Block Diagram*

Results

FPGA Synthesis and Validation Results - The modified SoC was synthesized on a Xilinx Kintex-7 FPGA to validate its functionality in a real-world environment. The synthesized SoC on the Xilinx Kintex- 7 FPGA demonstrated stable operation under real- world conditions. The PPA comparison table of the ARM and RISC-V Swapped SoC is listed in the table 1.

Benchmark Results - We executed a series of performance benchmarks of Mibench suite in a bare-metal environment, focusing on key metrics such as instruction throughput, memory latency, and computational efficiency in terms of Instruction per cycle (IPC).

The results are shown in Figure 2. The IPC results showed that the CVA6 core achieved competitive performance demonstrating the system's capability to perform efficiently and reliably under practical conditions.



- *Figure 2 - Benchmark Results*

PPAs Comparison of ARM SoC and Swapped-Core SoC

Metric	ARM SoC	Swapped-Core SoC
No. of LUTs Used	108,797	89,910
Power (W)	2.487	2.489
Delay (ns)	11.390	11.880

- *Table 1*

Conclusion

- The CoreSwap project demonstrates the feasibility of replacing a proprietary ARM core with an open-source RISC-V core in an existing SoC while maintaining full system functionality.
- Implemented verification strategies ensured correctness at multiple levels, from core-level ISA compliance to full system operation highlighting the importance of a robust verification process in enabling the adoption of RISC-V in diverse SoC environments.

For more Information, visit 10xEngineers website.

References

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